In the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Cancelled)

2. (Previously Presented) An ESD protection circuit comprising:

a substrate;

a transistor formed on the substrate;

a first insulating film formed on the substrate inclusive of the transistor and having a first contact hole to an input terminal of transistor;

a buffered layer formed on the first insulating film inclusive of the first contact hole and electrically connected to the input terminal for acting as a resistor;

a second insulating film formed on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer; and,

a pad formed on the second insulating film inclusive of the second contact hole and electrically connected to the buffered layer, for discharging

static electricity from said pad, through the buffered layer, and through said transistor to ground.

3. (Previously Presented) A method for fabricating an ESD protection circuit, comprising the steps of:

(1) forming a transistor on a substrate;

(2) forming a first insulating film on the substrate inclusive of the transistor and having a first contact hole to an input terminal of the transistor;

(3) forming a buffered layer in the first contact hole and the first insulating film in the vicinity of the first contact hole;

(4) forming a second insulating film on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer; and,

(5) forming a pad both on the second contact hole and the second insulating film in the vicinity of the second contact hole, for discharging static electricity from said pad, through the buffered layer, and through said transistor to ground.

4. (Original) A method as claimed in claim 3, wherein the buffered layer is formed of polysilicon.

5. (Original) A method as claimed in claim 3, wherein the buffered layer is formed of a silicide.

6. (Cancelled)